CENTRE FOR DEVELOPMENT OF ADVANCED COMPUTING

Walk-in Advertisement No. C-DAC/Noida/02/December/2023 **Dated: 20-12-2023**

Centre for Development of Advanced Computing (C-DAC), is a Scientific Society of the Ministry of Electronics and Information Technology, Government of India. CDAC Noida is currently handling various projects of national importance in Digital health, E-Governance, Transportation & Transit applications, Communication, Cyber Security, Artificial Intelligence/ML/DL and analytics, Smart Card-OS Development, etc. We are looking for bright & result oriented professionals for the following positions in various projects for appointment on **purely Contract basis for the following positions:-**

1. **Program Manager**
2. **Project Engineer**

Interested and eligible candidates are required to appear for a Walk-in interview as per the schedule below:-

Date	Position	Numbers	Registration Timings
04.01.2024 (Thursday)	Program Manager(Project Management & Implementation/Electronics & VLSI Design)	02	10 am to 12 noon only
04.01.2024 (Thursday)	Project Engineer (Quantum Computing, Applied AI/ML & VLSI)	05	
05.01.2024 (Friday)	Project Engineer (JAVA,J2EE Software/ Web Application Development/C, C++)	55	

Candidates are required to **download the blank Application Proforma** and carry the duly filled application form affixed with latest passport size photograph, attested copies of documents such as proof of age, qualification, experience, caste, etc and reach the venue on the stipulated date. Candidates who register themselves at the venue between 10 am to 12 noon will be allowed to attend the interview.

All the above posts are purely on contract basis on consolidated emolument initially for a period of 03 (THREE) year or co-terminus with the project whichever is earlier. However, term of contract may be considered for extension for a further period of another three year not more than two years at a time based on performance of the incumbent and requirement of the project. However, C-DAC, Noida reserve the right to terminate the Contract even during the contract period or extended contract period without assigning any reason after giving 45 days prior notice, or salary in lieu thereof. The selected candidates will be eligible to apply for different/higher post, on contract on consolidated pay basis, against internal notifications issued from time to time. Details of position, age, qualification, essential experience and eligibility criteria are mentioned below:-

Date of Interview: 04th January, 2024 (Thursday)	
Position	**Program Manager**

Specialization/Domain	Project Management and Implementation/ Electronics & VLSI Design
No. of Positions (indicative only)	02
Essential Qualification	• 1st Class (60%) B.E/B. Tech./MCA or equivalent degree in relevant disciplines** or • Masters in Technology (M. Tech)/Masters in Engineering (M.E) in relevant disciplines** or • Ph. D in relevant disciplines**
	****Relevant Disciplines:** Computer Science/IT/Electronics & Communication Engineering/Artificial Intelligence/Software Engineering/Machine Learning/Data Science/Blockchain/Cloud Computing/ Electronics & Instrumentation/Bioinformatics/Computer & Information Science/Electronics & Nanotechnology/Electronics & Telecom Engineering/Geo Informatics Engineering/Information Science & Engineering/Mathematics & Computing/Telecommunication Engineering
Post Qualification Experience	• 9-15 years of post qualification relevant work experience to the job description
Skill sets	• Candidate should have experience in handling projects in VLSI Semiconductor Design Organizations. • Candidate should also have experience of handling Govt. Project and should be experienced in leading Projects Management Units for Govt Schemes/ Projects with management of various stakeholders. • Candidates should have knowledge of Project Management practices. Knowledge of Agile Project Management Practices is desirable. PMP/ PMP Trained candidate would be preferred.
Job Profile	• Lead the execution and end-to-end implementation of the Design Linked Incentive (DLI) Scheme; • Develop a work plan for overall implementation of the Scheme in collaboration with CEO/ Head of DLI Scheme; • Direct interface with various Government, private/public stakeholders; • Management of evaluation of Proposals received through the Semiconductor Industries. Involved in complete end-to-end management with the industries, evaluation and verification of the proposals, seeking approval of competent authority for valid

	proposals; • Take a lead in and monitor the implementation of the Scheme in a systematic manner through developing a monitoring framework to assess and monitor overall progress of the Scheme on a regular basis; • Managing interdependencies and coordination across projects to ensure that information relating to project deliverables, risks and issues are effectively communicated between stakeholders and that key performance indicators are monitored and evaluated; • Mentoring and supervision of team under PMU /Project Associate / Project Assistant; • Maintaining file record of all the files under the Schemes. • Managing tasks with Financial and technical Evaluation teams. • Preparation of Agenda, Minutes of Meetings, Draft etc. Handling of queries of various stakeholders. • Coordinate the development, implementation and monitoring of project activities and schemes; • Provide support and inputs for Workshops/Road shows and visits. • Support PMU in preparing reports and related documents through provision of required inputs, as requested. • Any other work related to the Scheme Implementation.
CTC per Annum	*₹ 17.52/- lakhs per annum based on the post qualification relevant experience as per C-DAC norms
Age	Maximum 50 years as on 31.12.2023

Date of Interview: 04th January, 2024 (Thursday)	
Position	**Project Engineer**
Specialization/Domain	VLSI
No. of Positions (indicative only)	**03**

Essential Qualification	• 1st Class (60%) B.E/B. Tech. in Computer/ Electronics/ Electronics & Telecommunication/ Communication /Electrical & Electronics OR • ME/M. Tech in Computer/ VLSI /Electronics/ Electronics & Telecommunication/ Communication / Electrical & Electronics
Minimum Post Qualification Experience	• 2-4 years of post-qualification relevant experience relevant to the job description
Skill sets	• Knowledge and familiarity with Linux OS and related development • Verilog HDL coding and Verification • EDA tools Mentor/Cadence/Synopsys • Working Knowledge in latest Xilinx/Intel FPGA tools and frameworks • Working Knowledge in AI/ML tool Ecosystem for Xilinx/Intel devices • Working Knowledge in Synthesis using Programmable SoC & FPGAs • Working Knowledge in Front end VLSI/FPGA design.
Job Profile	• Architecture/Specifications for the relevant block, micro-architecture of one or more block. • Implement a specification using RTL coding techniques and best practices • FPGA Design and implementation and IP Core Prototyping. • Design implementation on latest Xilinx/Intel FPGA Unified development platform • Full-chip simulation, Timing Analysis, Design Verification plus debug • System level Validation • Technical Documentation.
CTC per Annum	*₹8.22-₹8.94/-lakhs per annum based on the post qualification relevant experience as per C-DAC norms
Age	Maximum 35 years as on 31.12.2023

Date of Interview: 04th January, 2024 (Thursday)	
Position	**Project Engineer**
Specialization/Domain	Quantum Computing, Applied AI/ML

No. of Positions (indicative only)	**02**
Essential Qualification	• 1st Class (60%) B.E/B. Tech in Mathematics & Computing/Computer Science/ Quantum Information/Quantum Technology/ Artificial Intelligence or • Masters in Technology (M. Tech)/Masters in Engineering (M.E) in Mathematics & Computing/Computer Science/ Quantum Information/Quantum Technology/ Artificial Intelligence or • Ph.D in Quantum Computing/Quantum Informatics/Quantum Data and relevant fields
Minimum Post Qualification Experience	• 2-4 years of post-qualification relevant experience relevant to the job description
Skill sets	• Understanding of Quantum mechanics and Machine learning/Deep learning • Knowledge of Quantum computing like Qiskit, pennylane, Qsim, Amazon Braket. • Good understanding of machine learning platforms like tensorflow, pytorch, caffee • Knowledge of C/C++, Python • Experience in implementation/timing of machine learning, quantum circuits and quantum gates. • Knowledge on ML/ AI, HPC, GPU • Knowledge and Familiarity with Linux OS and related development
Job Profile	• Implement Quantum circuits on different H/W and simulator stacks. • Implementation of Hybrid Quantum Machine Learning algorithms. • Development of tools for quantum machine learning and quantum simulation • Development of the Quantum Simulators/Testing Frameworks/Software Interfaces and Integration. • Development/Optimization of QC Algorithms and POC application and other use cases
CTC per Annum	*₹8.22-₹8.94/-lakhs per annum based on the post qualification relevant experience as per C-DAC norms
Age	Maximum 35 years as on 31.12.2023

Date of Interview: 05th January, 2024 (Friday)	
Position	**Project Engineer**
Specialization/Domain	JAVA,J2EE Software/ Web Application Development/C, C++
No. of Positions (indicative only)	**55**
Essential Qualification	• 1st Class (60%) B.E/B. Tech. /MCA or equivalent degree in relevant disciplines**
	****Relevant Disciplines:** Computer Science/IT/ Computer Applications/Electronics /Electronics & Communication Engineering/Artificial Intelligence/Software Engineering/Machine Learning/Data Science/Blockchain/Cloud Computing/ Electronics & Instrumentation/Bioinformatics/Computer & Information Science/ Electronics & Nanotechnology/Electronics & Telecom Engineering/Geo Informatics Engineering/Information Science & Engineering/Mathematics & Computing/Telecommunication Engineering/Electrical & Electronics/ VLSI
Minimum Post Qualification Experience	• 2-4 years of post-qualification relevant experience relevant to the job description
Skill sets	• Languages: Java, J2EE • Web Technologies: JavaScript, AJAX, JSP, Soap/ Rest Bootstrap, SCSS and JSON, jQuery, HTML 5.0, Angular/React JS • web services, Micro-services • Frameworks: Spring, Spring Boot, MicroServices, Security + Form Filter, OAuth 2, Hibernate and Web services • Database: PostgreSQL/Oracle/MySQL, DB Visualizer • NoSQL (Mongo/Casandra), Apache Kafka, Spark • Version Controller: SVN, GitHub or Code Hub, Maven • IDE: JBoss, My Eclipse Blue, JDeveloper, Web sphere Application Server and Maven (Eclipse) • Application / Web Servers: JBoss/ OC4j/ Web sphere/ Jenkin/ WildFly Console Dockers

	• Tools: New Relic, Fortify • Methodologies: Agile/Scrum and DevOps tools-CICD • Testing Frameworks: Junit, Mockito & Selenium web (Optional) **OR** • C/C++/Microcontroller programming/Cryptography • Designing, developing, coding, testing, and debugging for embedded devices and systems. • Hands-on development and troubleshooting on embedded targets • Experience of translating the functional specifications into Architecture and Design and disseminating the same to teams. • Familiarity with software configuration management tools, defect tracking tools, and peer review • Proficiency in Microsoft Word, Excel, PowerPoint • Ability to communicate information, whether technical or non-technical to staff members in a clear and concise manner
Job Profile	• Mainly responsible for Design, Development & Implementation of Web applications • Candidate must have good experience in software engineering practices and have analytical abilities with quality approach towards the software design and development. • Good understanding of object-oriented programming concepts, Experience /Knowledge in Machine Learning & Android programming will be preferred for some assignments. • Maintenance and Management of web applications • Ensure secure coding practices in all developments • Collaborate with cross-functional teams to define, design, and ship new features **OR** • Design and implement software of embedded devices like PKI dongle, TPM etc. from requirements to production and commercial deployment. • Design, develop, code, test and debug firmware • Review code and design • Interface with hardware design and development • Hardware and Firmware Development • Engaging with end users/client, understand their requirements,

	capturing and translating the same into functional specifications to be used by the Architecture and Design teams. • Collaborate with development team and user/client to ensure that requirements are met • Following industry trends locally and internationally • Interact professionally with a diverse group; developers, Stakeholders, and subject matter experts
CTC per Annum	*₹8.22-₹8.94/-lakhs per annum based on the post qualification relevant experience as per C-DAC norms
Age	Maximum 35 years as on 31.12.2023

***C-DAC reserves the right w.r.t. to the pay to be offered to selected candidates based on the norms of C-DAC. Higher starting pay may be allowed to candidates possessing higher qualification or certifications namely like PMP, CISSP, etc.**

Instruction to Candidates:-

- Before appearing for the Walk-in interview the Candidates should read 'General Terms and Conditions' carefully.
- **Candidates are advised to appear against only one position**, accordingly, you must ensure your suitability for the position desired to appear in walk-in interview.
- Candidate should read all the eligibility parameters and ensure that he/she is eligible for the post before appearing for walk-in interview.
- Candidate should have a **valid email id and mobile no.** which should remain valid & active till the completion of selection process.
- **Candidates should bring** the complete application form along with a latest photograph affixed on it.
- **Candidates should also bring** original certificates and a **set of photocopy** of the following documents:-

1. Qualification Degree Certificates-Mark-sheets of 10th, 12th, Graduation, Post-Graduation along with consolidated mark sheets and degrees as applicable
2. Age Proof Document, ID Proof (PAN Card/ Aadhar Card)
3. Work Experience- Certificates (starting from first to last company, along with offer letters and experience certificates). Please bring document in respect of your present employment (latest salary slip and I-card).
4. Caste Certificates (in case of SC/ST/OBC)
5. Income & asset certificate {in case of Economically Weaker Section (EWS)}

- Candidates working in Central/ State Govt./ Autonomous Bodies/ PSUs are required to produce 'No Objection Certificate' from their parent organization.
- Candidates are advised not to carry your mobile/any such kind of gadgets during the interview.

Please Note:

The candidates are advised to visit C-DAC website regularly for notices/ information. Corrigendum/Extension/updates etc., if any, shall be published in our website **www.cdac.in** only.

General Terms & Conditions:-

Reservation:

- Reservation for SC/ST/OBC/EWS will be applicable as per the Govt. of India norms, as applicable to C-DAC.
- Candidate belonging to reserved categories should produce the certificates at the time of interview, issued by competent authority in the prescribed format as stipulated by Government of India, failing which such candidates will not be allowed to attend the interview against reserved posts and will not be allowed to claim the relaxations applicable in case of reservation.
- In case of candidates belonging to OBC category, certificate should specifically contain the clause that the candidate does not belong to creamy layer section.

Relaxation/ Age Limit

- Applicants belonging to the reserved category (SC/ST/OBC) / physically challenged/Ex-servicemen would be eligible for relaxations according to the Government of India norms.
- Government employees will be eligible for relaxation in age by 5 years including other age relaxations.
- C-DAC internal candidates also will be eligible for an age relaxation of 5 years including other age relaxations.
- The cut-off date for ascertaining the age and experience will be **December 31, 2023**.

Qualification:

- All the qualifying qualifications should be from AICTE/UGC approved/recognized University/Deemed University/Institutes. The courses offered by autonomous institutions should be recognized as equivalent to the relevant courses approved/recognized by Association of Indian Universities (AIU)/UGC/AICTE.
- Wherever CGPA/OGPA or letter (A, A+) grade in a qualifying degree is awarded, equivalent percentage of marks should be indicated in the application form as per norms adopted by the respective University/Institute. Please also obtain a certificate to this effect from University / Institute, which shall be required at the time of interview.

Experience:

- Only those experiences which are relevant and acquired after the passing date of the qualifying qualification will be considered. The decision of C-DAC in this regard will be final and binding.
- The period of experience rendered by a candidate as intern, trainee, research fellow, part time basis, visiting/ guest faculty will not be counted while calculating the valid experience for short listing the candidates for interview.

Important Notes:

- Management reserves the right to change/modify the selection process at any time, during the process, at its discretion. The decision of the management will be final and binding.
- The qualification and experience prescribed are the minimum requirements and possession of the same does not automatically make the candidates entitled for interview and selection processes. There will be an initial screening based on the academic and other parameters given in the resume and only those screened-in will be considered for further selection process.
- The management reserves the right to increase the minimum eligibility criteria, in the event of the number of applicants more, for any post(s) at its discretion. Candidates will be selected on the basis of their academic credentials, experience profile, performance in the interview and such other selection processes/parameters, as deemed fit by management.
- The number of vacancies indicated in the notification is tentative. CDAC reserves the right to increase or decrease the number of advertised posts at the time of selection. Further, CDAC also reserves the right NOT to fill any of the posts advertised. Also the posts are time bound and are purely contractual in nature for specified duration. The persons engaged on contract will not derive any right or claim to have a regular post in CDAC.
- **Canvassing in any form will be a disqualification for selection.**
- In case of internal candidates, please note that employees working in a particular post cannot apply for the same post in the same centre.
- In case of internal candidates, please note that the finally selected candidates will have to resign from the services and join the post as fresh employees.
- **C-DAC reserves the right to fill up the post or increase/decrease the number of posts or offer the lower post or even to cancel the whole or part of the process of recruitment without assigning any reason thereof.**
- **C-DAC reserves the right to cancel or introduce any examination/Personal Interview/Other selection process**. C-DAC also reserves the right to cancel/restrict/curtail/enlarge the recruitment process and/or the selection process without any notice and without assigning any reasons.
- **All the posts will be filled as per the Recruitment Rules or guidelines of C-DAC**.

- It is the responsibility of the candidates to assess his/her own eligibility for the post for which he/she is applying in accordance with the advertisement. **In case, it is found at any point of time in future during process of selection or even after appointment that candidate was not eligible as per prescribed qualification, experience etc, which could not be found at the time of selection due to whatever circumstances, his/her candidature/appointment shall be liable to be cancelled/terminated as case may be.**

- Choosing a particular department does not entitled the candidate to be appointed in the same department itself. If selected, management reserves the right to put candidate in any department.

- If required, the incumbents are posted at client site anywhere in India.

- No TA /DA will be provided for attending the walk-in interview.

- For any dispute, Courts at Noida/New Delhi will have the sole jurisdiction.